SPACEWIRE CODEC IP CORE UPDATE

Session: SpaceWire Components

Short Paper

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ABSTRACT

The University of Dundee developed the ESA SpaceWire IP core as the first step in the development of the SpaceWire router ASIC device, now available as Atmel standard part AT7910E. The core is used widely in many ESA contracts and is available from ESA for use on ESA projects, or under license from STAR-Dundee. To date the IP core, named "SpaceWire-b" by the ESA micro-electronics section, has been licensed for use in over 40 ESA projects [1].

The SpaceWire IP core was first released in 2003 and presented at the first SpaceWire seminar at ESTEC. Development of the IP core continued at the University of Dundee and three major revisions of the VHDL code have been released, adding extra features and fixing known issues.

1. INTRODUCTION

The SpaceWire [2] system is based on nodes connected together indirectly through routers or directly node to node via SpaceWire links. The role of a SpaceWire CODEC [3] in a system is the physical device which encodes and decodes the serial bit-stream over the SpaceWire links. The CODEC is implemented in technology independent RTL VHDL code. This paper presents a reference design example of the University of Dundee SpaceWire CODEC targeted at an Actel RTAX. The reference design is available with the new 2.03 release of the SpaceWire CODEC which is currently under review for release.

Actel Axcelerator RTAX devices are radiation tolerant version of the Axcelerator series of devices which are protected against single event latch-up and employ triple mode redundancy to resolve single event upsets in the internal FPGA fabric. Commercial grade AX devices are available, providing a prototyping path for lab testing.

2. SYSTEM DESIGN

An overview of the reference design is shown in Figure 1.

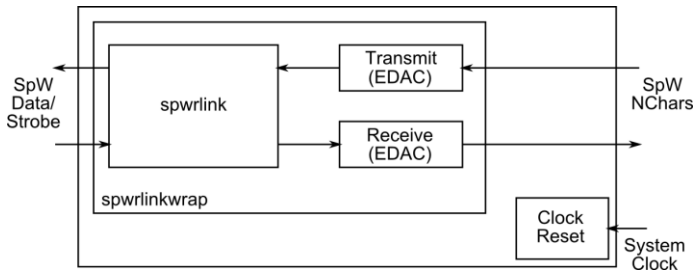

Figure 1 Reference Design Overview

The system clocks all the flip-flops except the receive clock domain. An HCLK global resource clock buffer is used for the system clock and is assigned an HCLKBUF primitive in the top level VHDL spwrlink_top.vhd file.

The system clock frequency is 100 MHz generating a 100 Mbps bit stream. The default 10 Mbps data rate is generated by enabling the transmitter flip-flops every three clock cycles. This is accomplished internally in the CODEC using the SYS_EN configuration of the transmit clock. The transmit rate can be further divided at run time using the TXRATE input signal.

A 100 MHz system clock with a 10 ns period is sufficient to give a valid 10MHz, 100 ns period, reference clock enable pulse for the timing blocks. In this case the CFG_SLOW_CE_SEL configuration signal is not set and the internal clock enable generator is used.

The receive clock domain is used exclusively inside the spwrlink block. The receive clock is attached to an internal CLKINT buffer. The receive clock frequency is 50 MHz for a 30 MHz input bit stream.

The system reset is a high fanout net which is internally routed on an RCLK global resource.

The transmit FIFO is implemented using an Actel AX memory block component (RAM64K36). In the Actel RTAX parts the same RAM block can be used with EDAC protection using an Actel smart design core. The FIFO control logic and buffer pointers are implemented in the FPGA fabric and are automatically protected from single event effects. The transmit FIFO RAM core is generated in Libero in the implementation section of this document. Scrubbing is not performed on the memory block.

The receive buffer is implemented using an Actel AX memory block component (RAM64K36). In the Actel RTAX parts the same RAM block can be used with EDAC protection using an Actel smart design core. The receive buffer RAM core is generated in Libero in the implementation section of this document. Scrubbing is not performed on the memory block.

3. RESULTS

The University of Dundee SpaceWire CODEC is a customisable model of the SpaceWire point to point serial interface specification, the SpaceWire standard. In this reference design example the CODEC is configured to run of a single clock in single data rate mode. A wrapper file is placed around the CODEC to include Actels EDAC

RAM blocks and global resource buffers. The main features and results of the reference design are given below.

- Error detection and recovery Actel Smart Design cores for input and output FIFOs.
- Single data rate transmitter implementation with one system clock and one receive clock.
- Step by step implementation guide using Actel Libero IDE, Synplify/Synplify Pro and Actel Designer.
- Layout guidelines and static timing analysis of the sensitive data recovery flip-flops.

Performance

The implementation is targeted to run at 100 MHz. The actual performance figures are listed in Table 2-1 Clock Performance and are discussed in section 8.3. Using the reference design a system clock frequency of 115.52 MHz can be achieved giving an output bit rate of 115.52 Mbps.

Clock	Requested	Achievable	Description
SYSCLK	100 MHz	115.52 MHz	System clock frequency.
RX_CLK	50 MHz	84.02 MHz	Receive clock frequency

Table 1 Clock Performance

Setting the Radiation setting in the Device Selection Wizard – Operating Conditions to 100Krad degrades the performance as follows

Clock	Requested	Achievable	Description
SYSCLK	100 MHz	112.18 MHz	System clock frequency.
RX_CLK	50 MHz	84.97 MHz	Receive clock frequency

Table 2 Clock Performance (100Krad degradation)

Resource Usage

The reference design is targeted to be as small as possible on the device. The area resource usage of the device is shown in Table 2-3 and the global buffer network resource usage is listed in Table 2-4.

Resource	Used	Available	Percentage Used	Description
R-Cells	508	6048	8.4%	Register elements
C-Cells	1095	12096	9.1%	Combinatorial elements
R+C-Cells	1603	18144	8.8%	Combined total
RAM	2	36	5.5%	Internal RAM blocks
IO	74	198	37.3%	Input output pads.

Table 3 Resource Usage

Net	Global	Fanout	Description	Inferred
i_sysclk_buf	HCLK	434	System clock	No
i_rclk_rst_n	RCLK	344	System reset	No
spwrlinkwrap_1/spwrlink_1/RX_RST_N_buf	RCLK	75	Receiver Reset	Yes
spwrlinkwrap_1/spwrlink_1/RX_CLK_buf	RCLK	114	Receive Clock	Yes

Table 4 Global network resource usage

Estimated Power Consumption Using the Smart Power estimation tool the following power estimations.

Parameter	Power (mW)	Percentage
Total Power	181.09	-
Static Power	97.01	53.6 %
Dynamic Power	84.08	46.4 %

Table 5 Power Estimation

4. CONCLUSION

The SpaceWire CODEC RTAX reference design is capable of achieving a 100 Mbit/s data rate using error recovery and detection FIFOs. The design has been proven using the Axcelerator commercial packages running at 100 Mbit/s in the lab. The latest version of the SpaceWire CODEC and the Actel reference design will be available after internal review by ESA and further testing of the design will be performed to achieve a 200 Mbit/s double data rate design. The core is used widely in many ESA contracts and is available from ESA for use on ESA projects, or under license from STAR-Dundee for non ESA contracts.

5. REFERENCES

[1] http://www.esa.int/TEC/Microelectronics/SEMKBWSMTWE_0.html, ESA IP Cores Usage Statistics, Updated on 8th Jan 2008

[2] ECSS, “SpaceWire: Links, nodes, routers and networks”, ECSS-E50-12A, January 2003

[3] "The SpaceWire Codec", C. McClements, S. Parkes and A. Leon, ISWS International SpaceWire Seminar 2003 (2003), pp.139-146. Noordwijk, The Netherlands, 4-5 November.